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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,896	01/30/2004	Makoto Terui	030712-23	5698

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/766,896	TERUI, MAKOTO
	Examiner	Art Unit
	Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *17-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 01-30-04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election without traverse of Group I, claims 1-16 in Paper No. 2 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

3. Claims 1-5 and 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger (US Pat. 5111278) in view of Maeda et al. (US Pat. 6582991) and Lin et al. (US Pat. 2002/0122244).

Regarding claims 1-5, 11, 12, 15 and 16, Eichelberger discloses a high density/highly integrated module (HDM) comprising a plurality of integrated circuit (IC) chip elements/components for high frequency/high performance applications, the IC chip element/component comprising:

- a substrate/base plate (112 in Fig. 8)
- the plurality of IC chip elements/components (106 in Fig. 7 and 8), the IC chip elements/components including active chip elements being formed in an array and being isolated from each other (see Fig. 8)

- electrodes/pads (not numerically referenced- see pads on 106 in Fig. 7 and 8) for electrically connecting the plurality of IC chip elements/components to an external source on top/bottom sides of the HDM through conventional contacts such as solder bumps (not numerically referenced in Fig. 8; Col. 3, lines 15-19), and
- the plurality of IC chip elements/components being selectively connected by metallization/second wiring on the encapsulating/insulating and through vias (see 80 in Fig. 5 and 116 in Fig. 8)

(Fig. 7 and 8; Fig. 2-8; Col. 15, line 45- Col. 19, line 35; Col. 1-19)

Eichelberger fails to teach the HDM comprising a plurality of passive elements/components, the passive elements/components being formed on the substrate by metal wires.

Maeda et al. teach a multichip module (MCM) having IC chip elements/components wherein the chip components include a variety of active and passive components (300 and 200 respectively in Fig. 2) wherein the passive component types include conventional resistor, capacitor, etc. each component having respective specifications (resistance, capacitance, inductance, quality factor, etc.), values and dimensions to provide the desired application requirements (Col. 13, lines 20-35). Furthermore, the elements/components include those of the same or different types (see Fig. 18, 19, etc.) as per application requirements (Col. 28, line 33- Col 30,

line 15) and the active and passive components being selectively connected by metallization/second wiring/pad-to-through hole wiring (see 122 in Fig. 2; Col. 13; lines 1-35).

Lin et al. teach a MCM having a variety of conventional passive devices/chip components (644 in Fig. 11A) including capacitor, inductor, etc. wherein the inductor and the capacitor are formed on a substrate by spirally disposed metal pattern/wires and conventional capacitor configuration including parallel wiring layers/electrode layers respectively (see 642a in Fig. 11A and Fig. 10B respectively; section 0072). Lin et al. further teach the chip components/passive devices being formed/diced from a wafer using a conventional wafer scale processing (sections 0006-00010).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the plurality of passive elements/components, the passive elements/components being formed on the substrate by metal wires as taught by Maeda et al. and Lin et al. so that the desired device integration and performance can be achieved and the component processing can be simplified in Eichelberger's HDM.

Regarding claims 13 and 14, Eichelberger, Maeda et al. and Lin et al. teach the entire structure as applied to claim 1 above, wherein Eichelberger further teaches:

- a plurality of encapsulating/insulating/protective layers (see 42 in Fig. 2) layers, the encapsulating/insulating covering the plurality of IC chip

elements/components and the encapsulating/protective film on the encapsulating/ layer and having openings (see the top layer 42 in Fig. 2)

- wherein the pads/electrodes/first electrodes (not numerically referenced- see pads on the IC chips in Fig. 2 and 8) that are formed on the insulating layer are connected to the plurality of IC chip elements/components and exposed through the openings in the insulating/protective film (see Fig. 8), and
- second electrodes/pads (see 24/32 in Fig. 2) being electrically connected to the pads/first electrodes, the second electrodes/pads being covered with a resin/substrate layer expect for the exposed part thereof (see Col. 9 and 10)

4. Claim 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger (US Pat. 5111278), Maeda et al. (US Pat. 6582991) and Lin et al. (US Pat. 2002/0122244) as applied to claim 1 above and further in view of Panella et al. (US Pat. 6853559).

Regarding claims 6-10, Eichelberger, Maeda et al. and Lin et al. teach the entire structure as applied to claims 1-5 above, except the plurality of passive elements being divided into a plurality of groups having mutually different specifications or groups including high and low frequency specifications.

Panella et al. teach an IC system integration comprising active/passive IC chips/components including resistor, capacitor, etc. wherein the chips/components include those having high/low frequency specifications, the system configuration further include the components being configured/divided into groups including high and low frequency specifications to provide the desired power/signal and performance requirements and improved electromagnetic interference (EMI) protection and thermal management (see col. 2, 5, 9, 22-28; Fig. 1-19).

Furthermore, the determination of parameters such as number of passive components, types, grouping according to the specifications including frequency characteristics and other performance parameters in a multichip packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired application requirements, module performance and reliability.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the plurality of passive elements being divided into a plurality of groups having mutually different specifications or groups including high and low frequency specifications as taught by Panella et al. so that the desired device integration, performance and reliability can be achieved in Maeda et al., Lin et al. and Eichelberger's HDM.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

NITIN PAREKH

04-27-05

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800